AD-A262 817

DTIC
ELECTE
MAR 18 1993
S C D

APPLIED RESEARCH, INC.

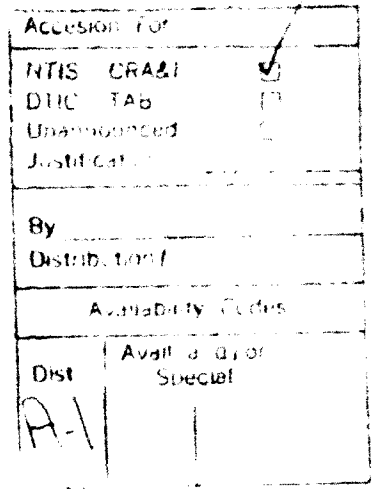
CAMMS PRE & POST PROCESSING PROTOTYPE DEVELOPMENT AND IMPLEMENTATION

Contract Number:
DAAH01-89-D-0069/0169
Subcontract Task 021
Final Technical Report

6700 ODYSSEY DR
P.O. BOX 11220
HUNTSVILLE, ALABAMA 35814-1220

Approved for Public Release
Distribution unlimited

ARI/92/R-034Z



CAMMS PRE & POST PROCESSING PROTOTYPE DEVELOPMENT AND IMPLEMENTATION

Contract Number:
DAAH01-89-D-0069/0169
Subcontract Task 021
Final Technical Report

Submitted To:
U.S. Army Missile Command-UAV
ATTN: *Dr. Richard Sims, AMSMI-RD-AS-SS*
Redstone Arsenal, AL 35898

Prepared by:
Applied Research, Inc.
P. O. Box 11220
Huntsville, AL 35814-1220
(205) 922-8600

September 30, 1992

93-05556

SECURITY CLASSIFICATION OF THIS PAGE

REPORT DOCUMENTATION PAGE

Form Approved
OMB No 0704-0188
Exp Date Jun 30 1986

1a REPORT SECURITY CLASSIFICATION Unclassified	1b RESTRICTIVE MARKINGS
2a SECURITY CLASSIFICATION AUTHORITY	3 DISTRIBUTION / AVAILABILITY OF REPORT
2b DECLASSIFICATION / DOWNGRADING SCHEDULE	
4 PERFORMING ORGANIZATION REPORT NUMBER(S)	5 MONITORING ORGANIZATION REPORT NUMBER(S) DI-SC-89-012, Task Order 21
6a NAME OF PERFORMING ORGANIZATION Applied Research, Inc. — 6b OFFICE SYMBOL (If applicable) ARI	7a NAME OF MONITORING ORGANIZATION U.S. Army Missile Command (MICOM)
6c ADDRESS (City, State, and ZIP Code) 6700 Odyssey Drive Huntsville, AL 35806	7b ADDRESS (City, State, and ZIP Code)
8a NAME OF FUNDING / SPONSORING ORGANIZATION U.S. Army Missile Command — 8b OFFICE SYMBOL (If applicable) AMSMI	9 PROCUREMENT INSTRUMENT IDENTIFICATION NUMBER
8c ADDRESS (City, State, and ZIP Code) ATTN: Dr. Richard Sims - AMSMI-RD-AS-SS	10 SOURCE OF FUNDING NUMBERS PROGRAM ELEMENT NO — PROJECT NO — TASK NO — WORK UNIT ACCESSION NO

11 TITLE (Include Security Classification)

CAMMS Pre & Post Processing Prototype Development and Implementation

12 PERSONAL AUTHOR(S)
G. Cantrell, R. Crump, A. Davis, M. Hose

13a TYPE OF REPORT	13b TIME COVERED	14 DATE OF REPORT (Year, Month, Day)	15 PAGE COUNT
Final Report	FROM 2/92 TO 9/92		

16 SUPPLEMENTARY NOTATION

17 COSATI CODES			18 SUBJECT TERMS (Continue on reverse if necessary and identify by block number)
FIELD	GROUP	SUB-GROUP	

19 ABSTRACT (Continue on reverse if necessary and identify by block number)

This final report describes the support provided by ARI to Dr. Richard Sims to help redesign the video A/D system for the CAMMS program. Included in the redesign is the capability to convolve two kernels up to 7x7 size across the input image, the ability to use EE PROMS for the target filter and to post process the output correlation surface.

20 DISTRIBUTION / AVAILABILITY OF ABSTRACT	21 ABSTRACT SECURITY CLASSIFICATION
☒ UNCLASSIFIED/UNLIMITED ☐ SAME AS RPT ☐ DTIC USERS	
22a NAME OF RESPONSIBLE INDIVIDUAL Roger L. Crump	22b TELEPHONE (Include Area Code) (205) 922-8600 x1042 — 22c OFFICE SYMBOL ARI

DD FORM 1473, 84 MAR — 83 APR edition may be used until exhausted. All other editions are obsolete.

SECURITY CLASSIFICATION OF THIS PAGE

TABLE OF CONTENTS

LIST OF FIGURES

1.0 INTRODUCTION

The current CAMMS Automatic Target Recognition(ATR) hardware contains a video A/D front end, a correlation engine and a microprocessor to post process the resulting correlation surface. This "minimal" configuration has been judged to be suitable for initial tests, however it is desired to be able to improve upon this configuration for later tests and analysis against more tactical targets.

Dr. Richard Sims has provided for ARI a description of the desired pre-processing prior to input to the correlation hardware and the post-processing desired after generation of the correlation surface. ARI has used this information to generate a preliminary design of the pre- and post-processing hardware. The initial implementation of this design is desired to be on an AT compatible prototype board and ARI has also supported the layout, prototyping and some fabrication of the desired circuits.

2.0 PRE-PROCESSING OVERVIEW

The preliminary design for the IBM/AT version pre-processor is detailed in the six pages of schematics in Appendix A. The intent of the IBM/AT version of electronics is to allow the user to capture RS170 images under computer control and access the preprocessed (convolved) results for analysis, evaluation and correlation reference filter synthesis. An example layout is shown in Appendix B.

The design processes the following features:

a) differential RS170 video input buffering.

b) sync and blanking generating phased to input video horizontal sync.

c) separate analog and digital grounds.

d) dual 8-bit video signal digitization.

e) real-time histogram computation.

f) microcontroller video "gain" control.

g) dual 7x7 pixel convolution with 8 bit convolution coefficients.

h) real-time modulus computation of convolver results.

i) telemetry video output of digitized video signal.

The processing of the RS170 analog video signal is depicted on page 1 of the schematics. U1 is used to differentially receive the analog video signal with a 75Ω input impedance. Components U2, U2, U8 and U13 perform the basic functions of extracting timing information from the input RS170 video. These functions include write pulse generation (WE), sync extraction (U8), pixel clock generation (U13), and pixel clock buffering and clock distribution (U15 and U16). Components U15 and U16 each show only one output being produced, PIXCLK and PIXCLK*. A total of ten outputs for each signal are available for satisfying the clock distribution requirements of this particular board. It is recommended that the exact number of outputs required of U15 and U16 be determined and defined in the prototype stage of development. Component U8 produces a 6.5 MHz pixel clock that is phased to the signal, CLAMP*, produced from the sync extraction chip, U8.

Component U10 provides the A/D processing required of the histogram chip, U11. Component U10 converts an RS170 signal to an 8-bit unsigned digital format. DC restoration occurs when the signal, CLAMPREG, is asserted. The A/D convertor will convert the DC restored signal spanning the voltage range of REFHI to REFLO. The signals REFHI and REFLO are to be held constant over the operating time of the preprocessor. Component U11 implements a real-time histogram function. The buffered results of U11 are accessible to the on-board micro-controller (U51).

Component, U9, converts the input RS170 video to digital format. Voltage references VREFHI and VREFLO are produced by the micro controller circuitry in a dynamic fashion to produce the variable "gain" feature of the design. The intent of the logic is to tailor the dynamic range of the 8-bit data bus, DVID, to the dynamic range of the input video signal. The data bus, DVID, is further input to the convolvers at U19, U26, U21 and U22.

The horizontal and vertical convolution functions are described on pages 2 and 3 of the electrical schematics. The horizontal convolution is implemented by U19 and U20. Component U19 produces the eight lines of delay required of the convolver at U20. The eight lines of delay are generated inside the component using 8-bit shift resisters configured to produce delays of 256 pixels per line. The delay line chip at U19 is required to be initialized by the micro controller. The component, U20 computes the real-time convolution of the data produced by component U19. The exact size of the convolution is determined when the micro controller preloads the convolution data. The device inherently implements an 8x8 pixel convolution. TO produce a 7x7 pixel convolution the coefficient registers in excess must be loaded with zeroes. The convolution output is produced as a 16-bit result on data bus DH.

The vertical convolution functions are depicted on page 3 of the schematics. The function and processing of the vertical convolution is the same as the horizontal convolution with the exception of the convolution coefficient values. The modulus computer (PDSP163301) computes the modulus of the output of the intermediate RAM buffer.

Page 4 of the schematics details the IBM/AT interface. The component at U27 decodes the address signals SA16 - SA19 and LA17 -LA23 to generate the chip selects required to read the 256x256 16-bit result of the preprocessing. The preprocessing result can be either memory mapped or IO mapped. The modulus RAM at U30-U35 contains the 256x256 16-bit result.

The intermediate memory storage and buffering required to implement the design is depicted on page 5 of the schematics. The right static RAM chips (CY7C191) implement an intermediate buffer between the horizontal and vertical convolution output and the modulus computation.

The micro controller circuitry is depicted on page 6 of the schematics is required to compute the dynamic digitization references VREFHI and VREFLO and the static references REFHI and REFLO for the dual A/D convertors on page 1 of the schematics. The D/A convertor at U54 converts the 8-bit digital word produced by the micro controller to an output voltage spanning 10V to 0V. The precision voltage reference at U52 produces a very precise 10V reference for the D/A convertor which will be stable under temperature. The micro controller at U51 is required for the following functions:

a) Static voltage references REFHI and REFLO.

b) Dynamic voltage references VREFHI and VREFLO.

c) 8-bit delay line initialization at U19 and U20.

d) Convolver coefficient loading and initialization at U20 and U21.

3.0 POST-PROCESSING

This section discusses the hardware necessary to calculate the mean and standard deviation (stdev) of the correlation output data. These computations will be made in real-time from the outputs of the barrel shifter.

The mean calculation involves summing the output values while the stdev involves summing the difference of the outputs and the mean. This often requires the mean calculation be completed before the stdev calculation can begin. However, if the sum of the outputs and the sum of the square of the outputs are calculated in parallel, they can be combined later to complete these calculations. This will allow the mean and stdev to be computed simultaneously with the stdev calculation completed with a few simple arithmetic operations. The square root operations will be performed by the DSP board.

The stdev equation can be manipulated, as shown below, and be expressed in terms of the sum of the outputs and the sum of the square of the outputs. This derivation shows that the stdev is computed by subtracting the square of the mean from the sum of the square of the outputs, divided by the number of outputs.

$$\sigma = \sqrt{\frac{\sum_{i=1}^{N} (x_i - \bar{x})^2}{N}}$$

$$\begin{aligned}
\sigma^2 &= \frac{1}{N}\sum (x_i - \bar{x})^2 \\
&= \frac{1}{N}\sum (x_i^2 - 2\bar{x}\, x_i + \bar{x}^2) \\
&= \frac{1}{N}\sum x_i^2 - \frac{2\bar{x}}{N}\sum x_i + \frac{\bar{x}^2}{N}\sum \\
&= \frac{1}{N}\sum x_i^2 - \frac{2\bar{x}}{N}\sum x_i + \frac{\bar{x}^2}{N}N \\
&= \frac{1}{N}\sum x_i^2 - 2\bar{x}\bar{x} + \bar{x}^2 \\
&= \frac{1}{N}\sum x_i^2 - 2\bar{x}^2 + \bar{x}^2 \\
&= \frac{1}{N}\sum x_i^2 - \bar{x}^2 \\
&= \frac{1}{N}\sum x_i^2 - \frac{\sum x_i}{N}\ \frac{\sum x_i}{N}
\end{aligned}$$

These computations are accomplished in hardware using two Multiply Accumulators (MACs) as shown in Figure 3.0-1. The internal accumulators must be sufficiently large as to allow the summations to be performed without overflow. The MAC used to compute the sum of the outputs requires a 32-bit accumulator. The MAC used to sum the square of the outputs requires a 44-bit accumulator. This is shown with the following calculations. These calculations are based on 256x256/16-bit 2's complement outputs. Although the outputs should neither be all max positive or all max negative, hardware was chosen to accommodate these worst case conditions. Mean and stdev estimations could be performed with current CAMMS hardware.

Sum of the outputs:

256x256x32768 = 2^8*2^8*2^15 = 2^31

256x256x32768x32768 = 2^8*2^8*2^15*2^15 = 2^44

A Cypress CY7C510 MAC is suggested for the first calculation. This part has a 35-bit accumulator and was previously used on the CAMMS A/D board for input image mean subtraction. Latching the upper 16-bits of the 32-bit output effectively performs a division by 256x256. This would immediately provide the mean value.

An LSI Logic L64032 MAC is suggested for the second calculation. This seems to be the only MAC available with an accumulator capable of storing the 44-bit results. This part has a 68-bit accumulator.

If the correlator input images are mean subtracted, then the output data should have zero mean. In this case only one MAC is needed and would compute the sum of the square of the outputs. However, a feature was added to the correlator hardware which clears all negative outputs. In this case, the mean output will be non-zero.

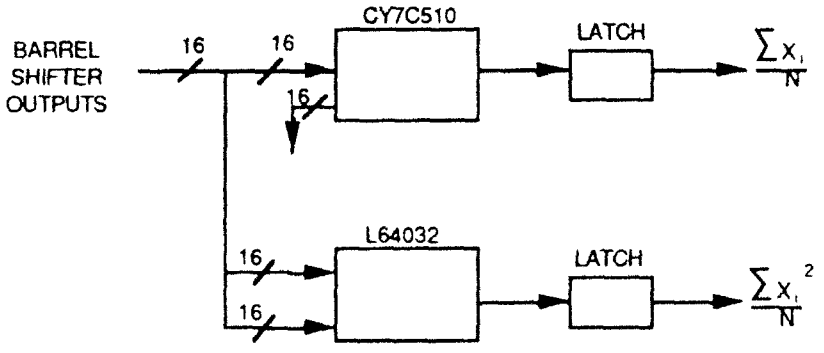


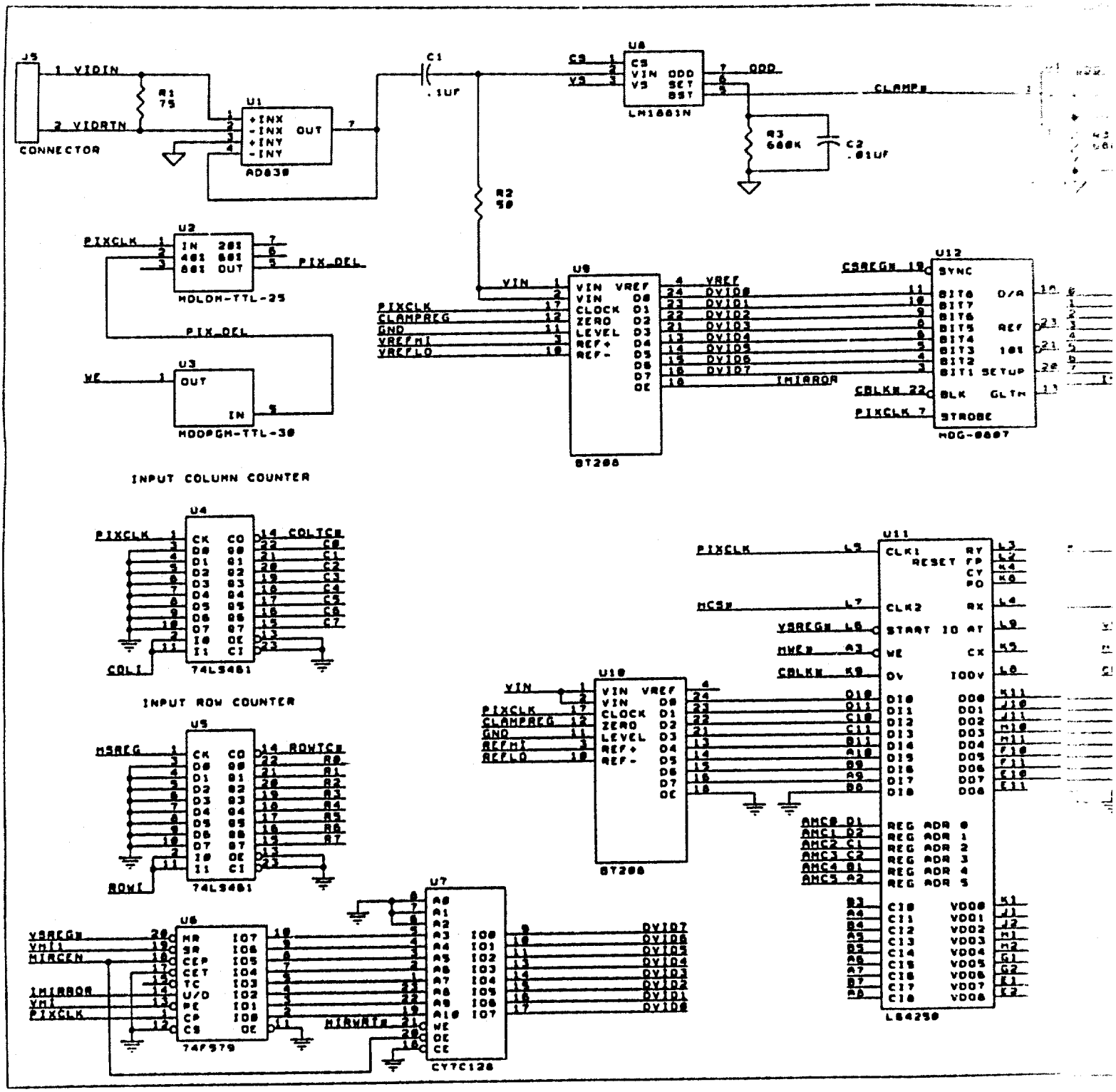
Figure 3.0-1 Computation of Mean and Standard Deviation

4.0 STATUS

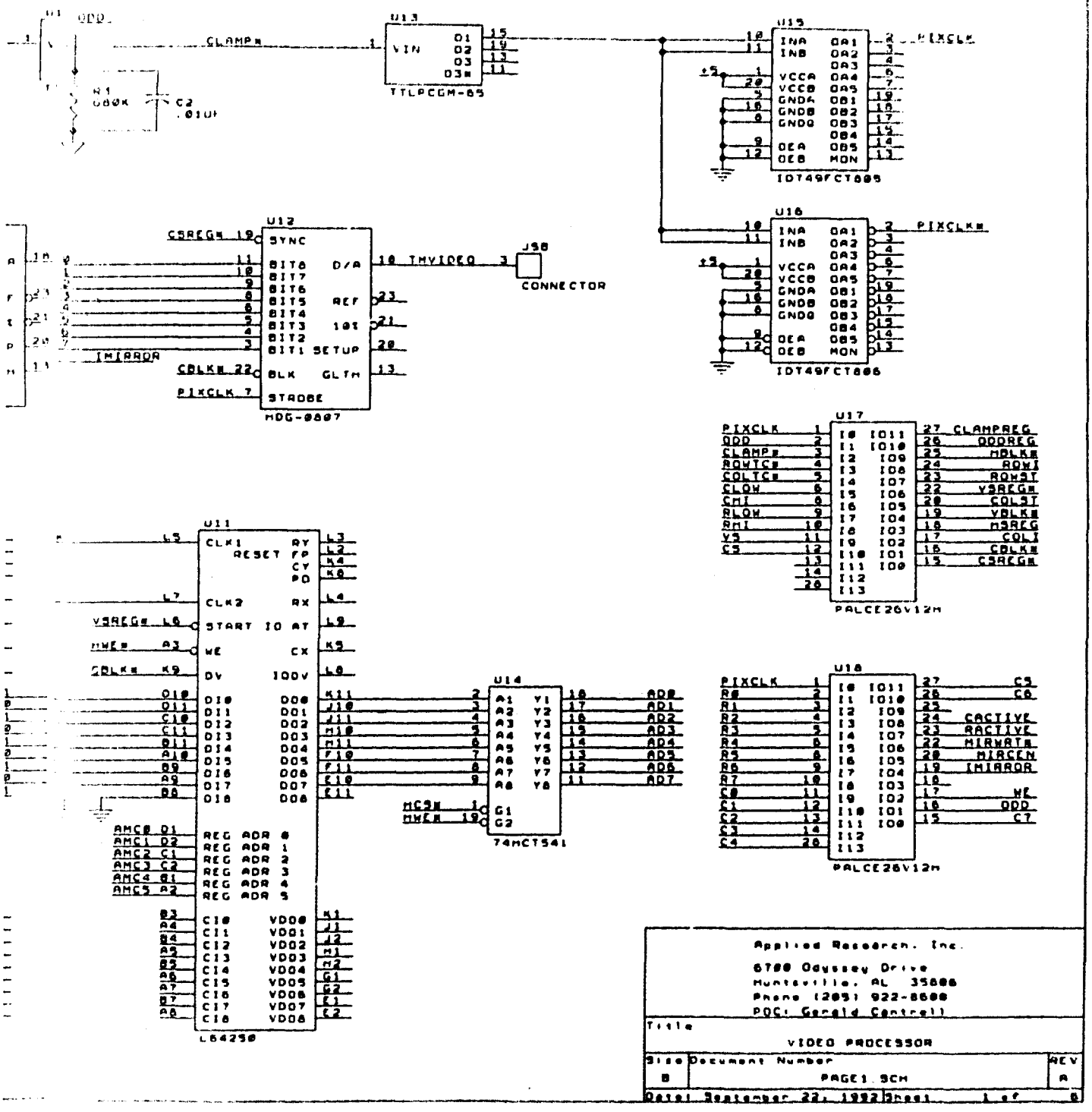
The schematics presented in this report will provide the means to initiate prototyping of the preprocessor. The firmware for the logic at U17, U18 U27, U56 and the PAL 20x10's on page 5 remain to be developed. Additionally the micro controller firmware for U51 must be further developed.

APPENDIX A

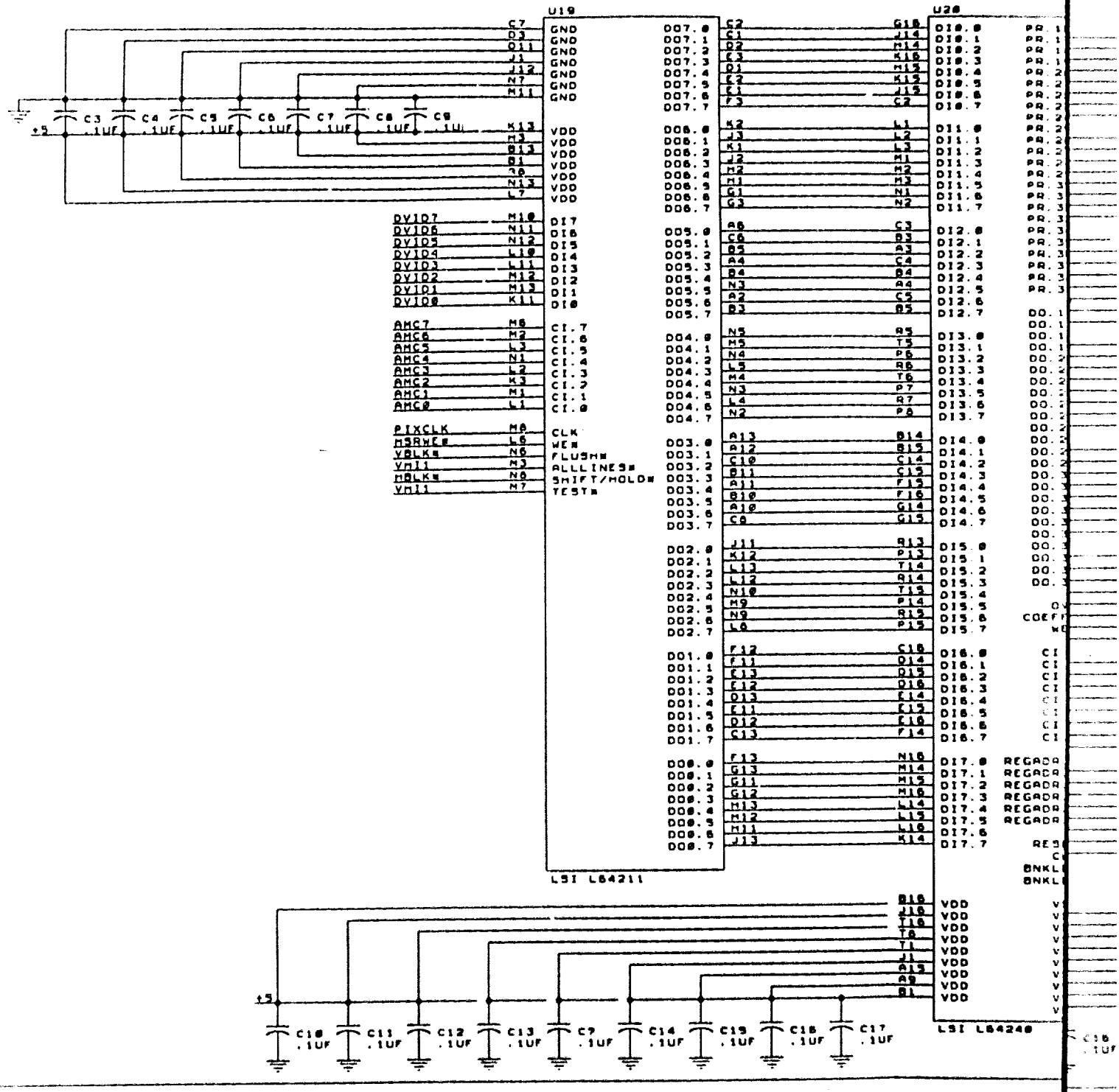
PREPROCESSOR IBM/AT ELECTRICAL SCHEMATICS

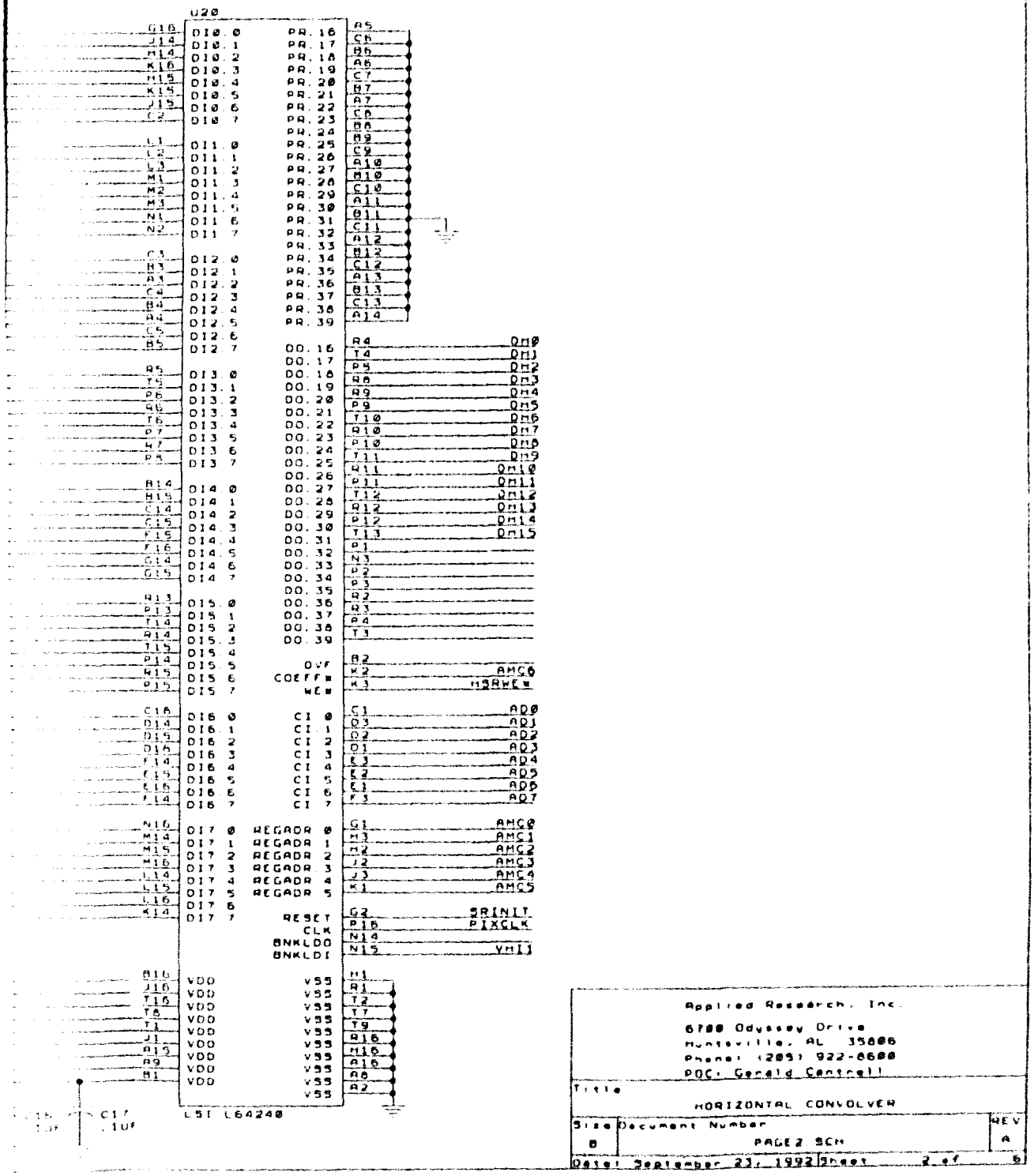

J5
1 VIDIN
2 VIDRTN
CONNECTOR
R1
75
U1
+INX
-INX
+INY
-INY
OUT
AD830
C1
.1UF
U8
CS
VIN
VS
ODD
SET
BST
LM1881N
CLAMPs
R3
680K
C2
.01UF
R2
50
U2
IN
2Q1
4Q1
8Q1
OUT
MDLDM-TTL-25
PIXCLK
PIX_DEL
U3
OUT
IN
MDDPGM-TTL-30
WE
INPUT COLUMN COUNTER
U4
CK
CO
D0
D1
D2
D3
D4
D5
D6
D7
I0
I1
OE
CI
74LS461
COLCTR
COL1
INPUT ROW COUNTER
U5
MSREG
ROWCTR
ROW1
U6
MR
SR
CEP
CET
TC
U/D
PE
CP
CS
I07
I06
I05
I04
I03
I02
I01
I00
74F579
VSREGs
VMI1
MIRCEN
IMIRROR
VMI
U7
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
WE
OE
CE
I00
I01
I02
I03
I04
I05
I06
I07
MIRWRTs
CY7C128
DVI07
DVI06
DVI05
DVI04
DVI03
DVI02
DVI01
DVI00
U9
VIN
VREF
CLOCK
ZERO
LEVEL
REF+
REF-
D0
D1
D2
D3
D4
D5
D6
D7
OE
VREFHI
VREFLO
GND
BT208
VREF
IMIRROR
U12
CSREGs
SYNC
BIT0
BIT7
BIT6
BIT5
BIT4
BIT3
BIT2
BIT1
BLK
STROBE
D/A
REF
181
SETUP
GLTN
CBLKs
MDG-8807
U10
U11
HCSs
VSREGs
MWEs
CBLKs
CLK1
RESET
CLK2
START
WE
CX
OV
IODV
RY
FP
CY
PO
RX
IO AT
D10
D11
C10
C11
B11
A10
A9
A8
D0
D1
D2
D3
D4
D5
D6
D7
D8
AMC0
AMC1
AMC2
AMC3
AMC4
AMC5
REG ADR 0
REG ADR 1
REG ADR 2
REG ADR 3
REG ADR 4
REG ADR 5
VD00
VD01
VD02
VD03
VD04
VD05
VD06
VD07
VD08
L84250

1A


U13
TTLPCOM-85
U15
IDT49FCT805
U16
IDT49FCT806
U12
MDG-0807
J98
CONNECTOR
U17
PALCE26V12H
U11
L64250
U14
74HCT541
U18
PALCE26V12H
Applied Research, Inc.
6780 Odyssey Drive
Huntsville, AL 35806
Phone (205) 922-8600
POC: Gerald Cantrell
Title
VIDEO PROCESSOR
Size B
Document Number
PAGE1.SCH
REV A
Date: September 22, 1992
Sheet 1 of 8

2A


U19
U20
LSI L64211
LSI L64240
+5
C3 .1UF
C4 .1UF
C5 .1UF
C6 .1UF
C7 .1UF
C8 .1UF
C9 .1UF
C10 .1UF
C11 .1UF
C12 .1UF
C13 .1UF
C7 .1UF
C14 .1UF
C15 .1UF
C16 .1UF
C17 .1UF
GND
VDD
DVID7
DVID6
DVID5
DVID4
DVID3
DVID2
DVID1
DVID0
AMC7
AMC6
AMC5
AMC4
AMC3
AMC2
AMC1
AMC0
PIXCLK
MSRWE#
VBLK#
VMI1
HBLK#
VMI1
CLK
WE#
FLUSH#
ALLLINES#
SHIFT/HOLD#
TEST#
REGADR

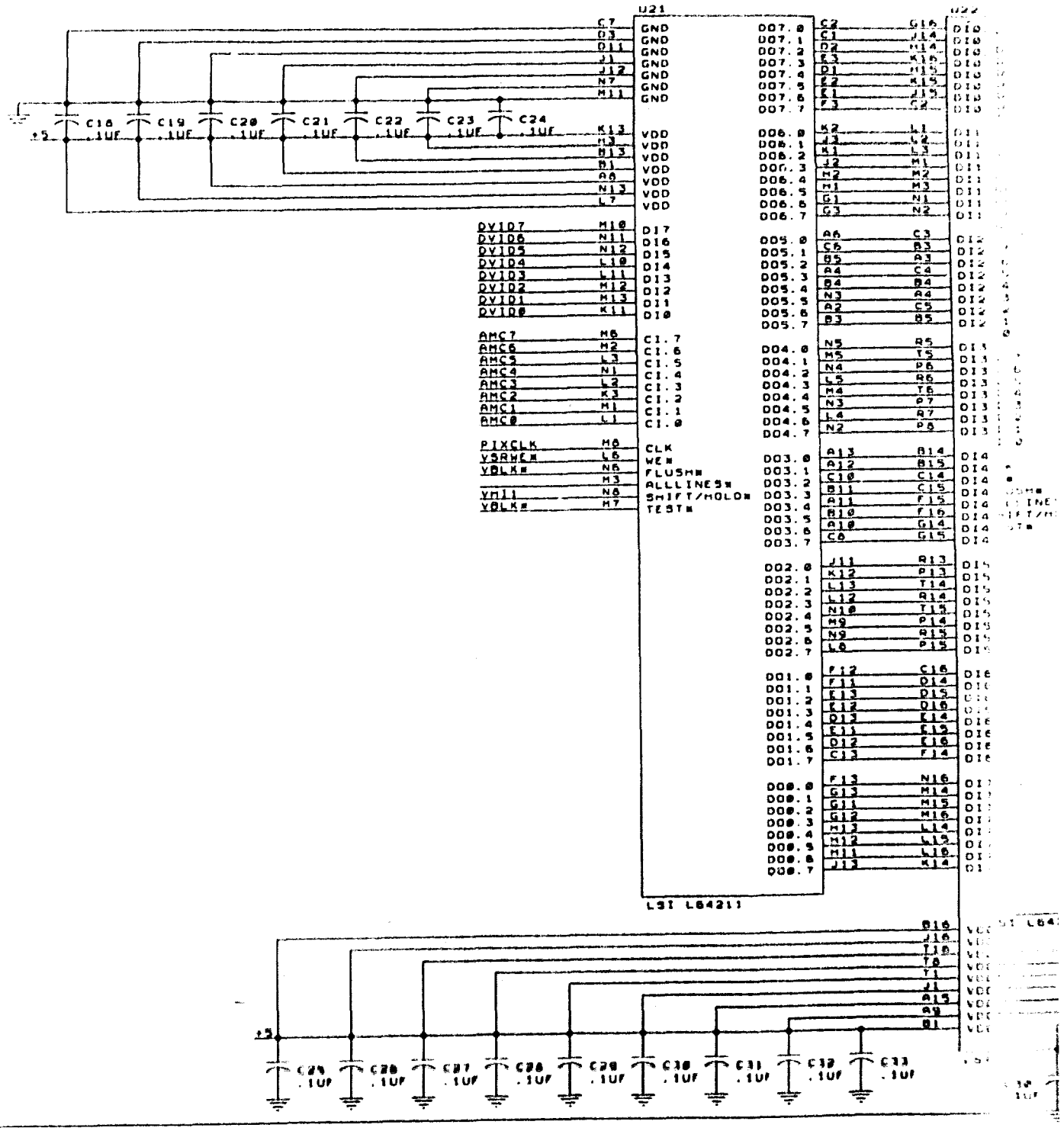


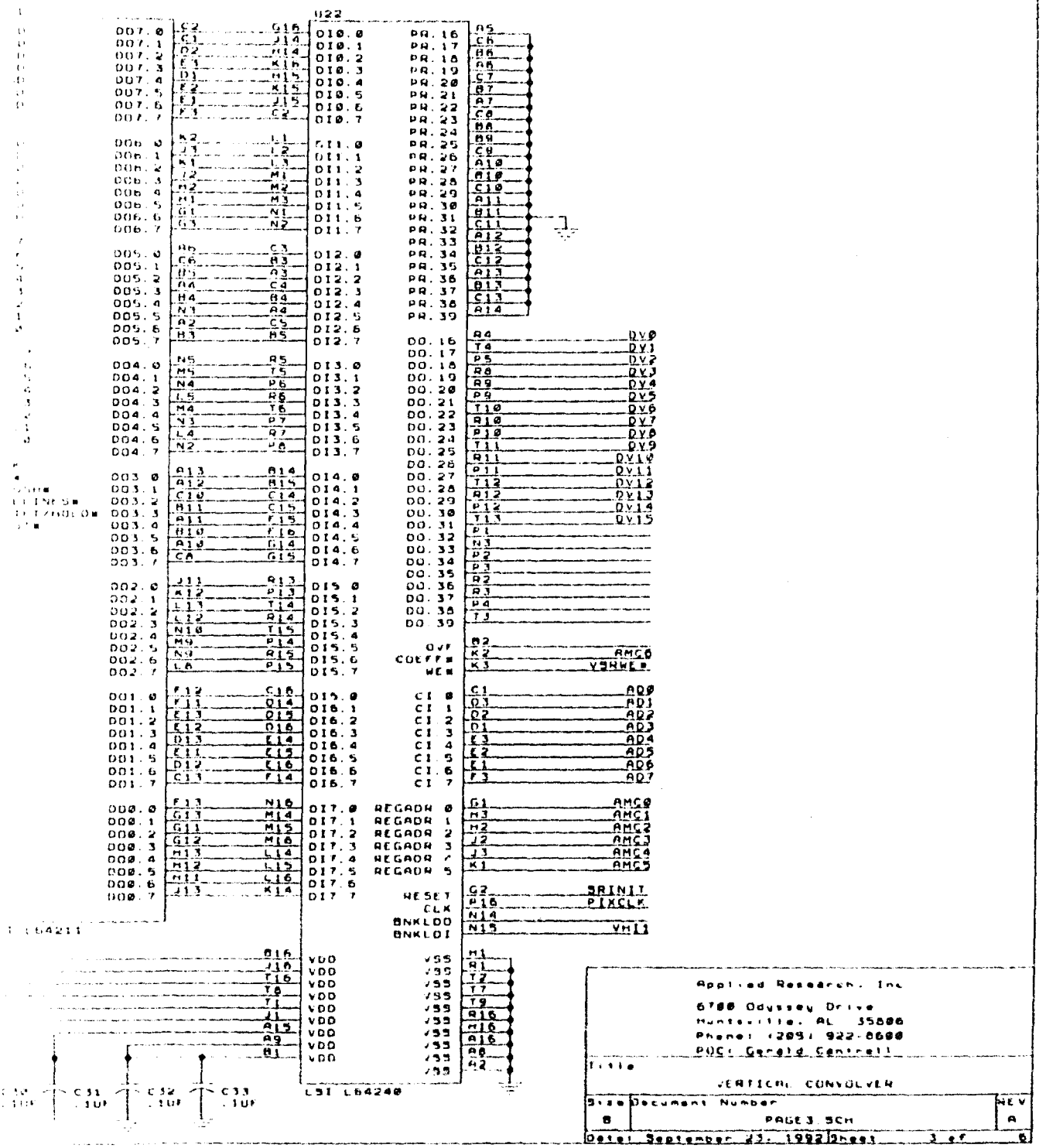
Applied Research, Inc.
6780 Odyssey Drive
Huntsville, AL 35806
Phone: (205) 922-6600
POC: Gerald Cantrell

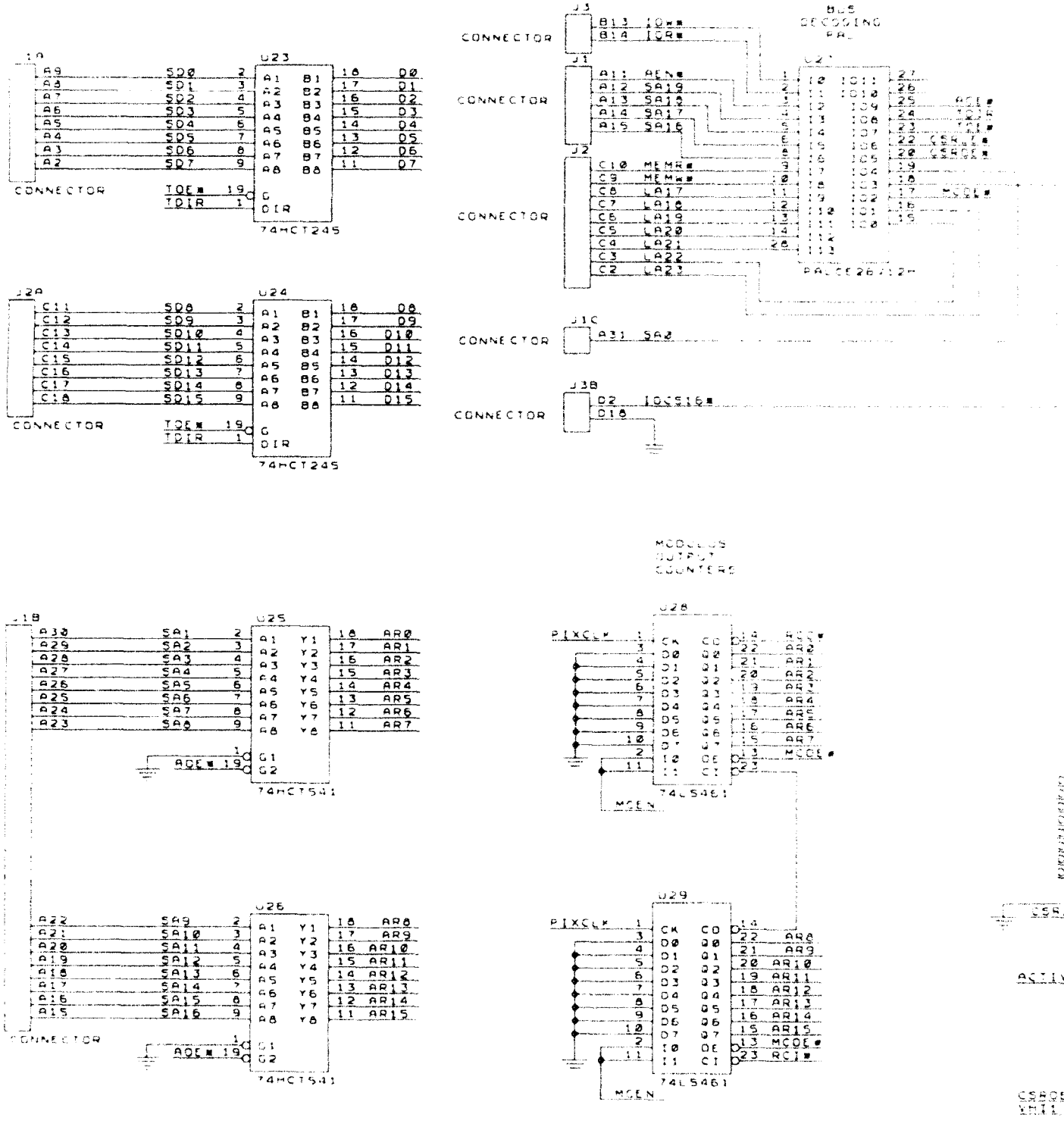
Title: HORIZONTAL CONVOLVER

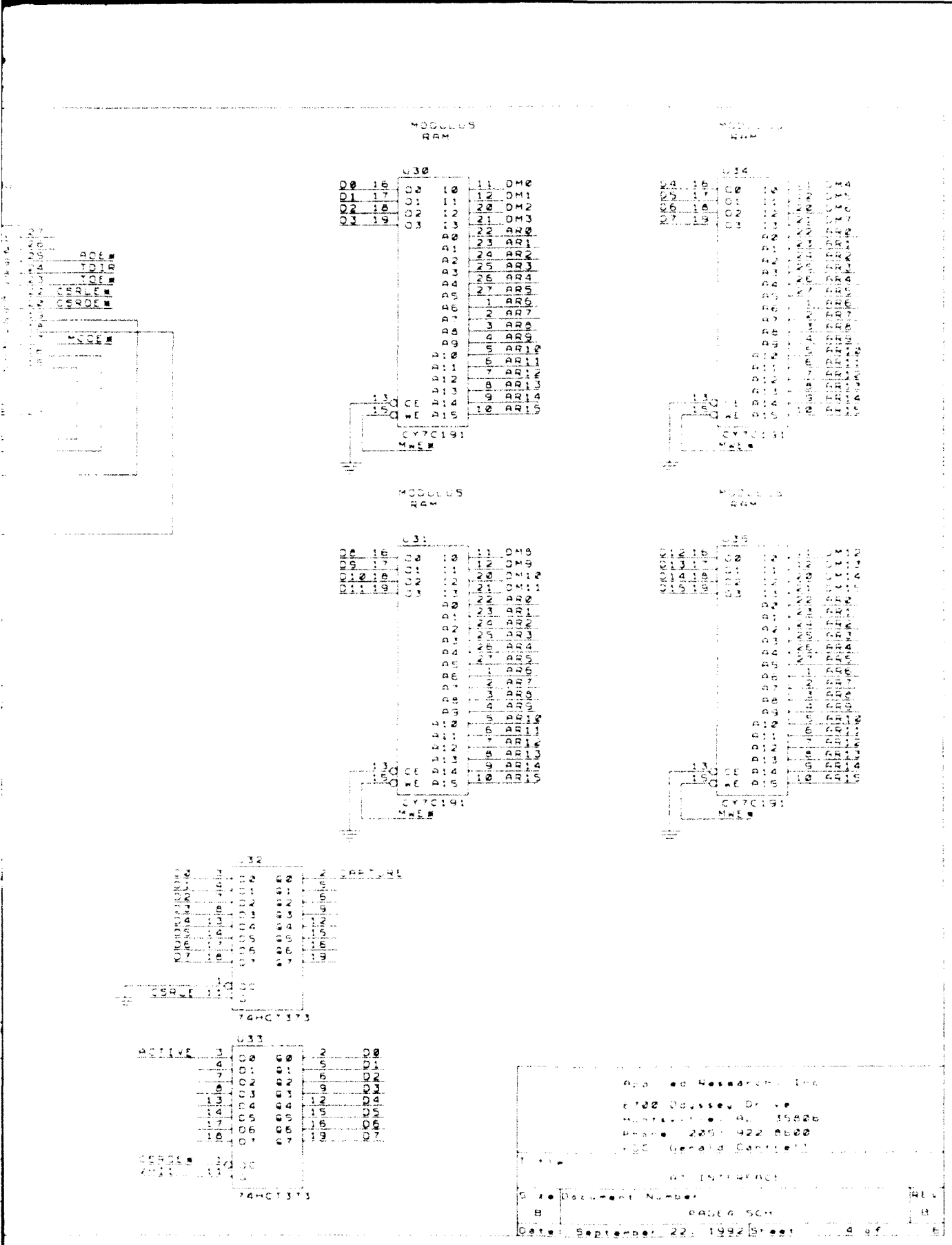
Size	Document Number	REV
B	PAGE2 SCH	A

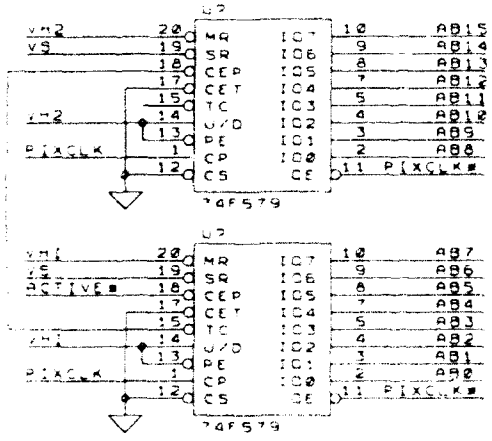
Date: September 23, 1992 Sheet 2 of 6

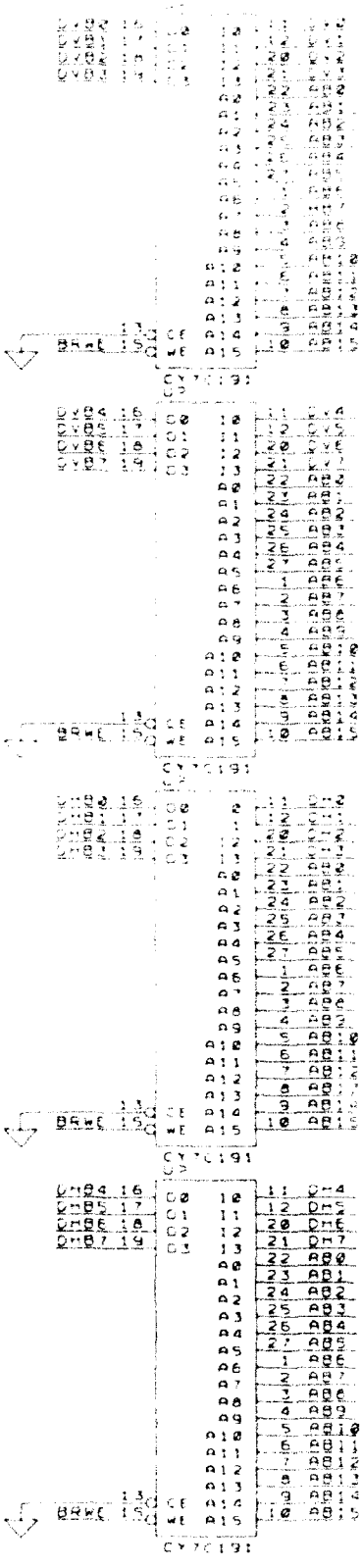

U21
LSI L64211
GND
VDD
CLK
WE#
FLUSH#
ALLLINES#
SHIFT/HOLD#
TEST#
C18 .1UF
C19 .1UF
C20 .1UF
C21 .1UF
C22 .1UF
C23 .1UF
C24 .1UF
C29 .1UF
C30 .1UF
C31 .1UF
C32 .1UF
C33 .1UF
+5

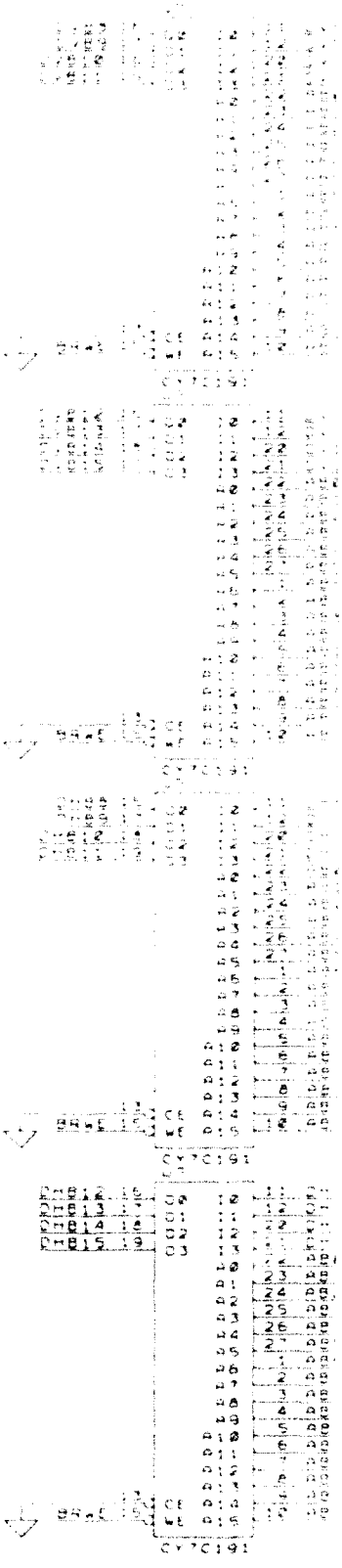

U22
LSI L64240
L64211
Applied Research, Inc.
6700 Odyssey Drive
Huntsville, AL 35806
Phone: (205) 922-8600
POC: Gerald Cantrell
Title
VERTICAL CONVOLVER
Size
B
Document Number
PAGE3.SCH
REV
A
Date: September 23, 1992
Sheet 3 of 6

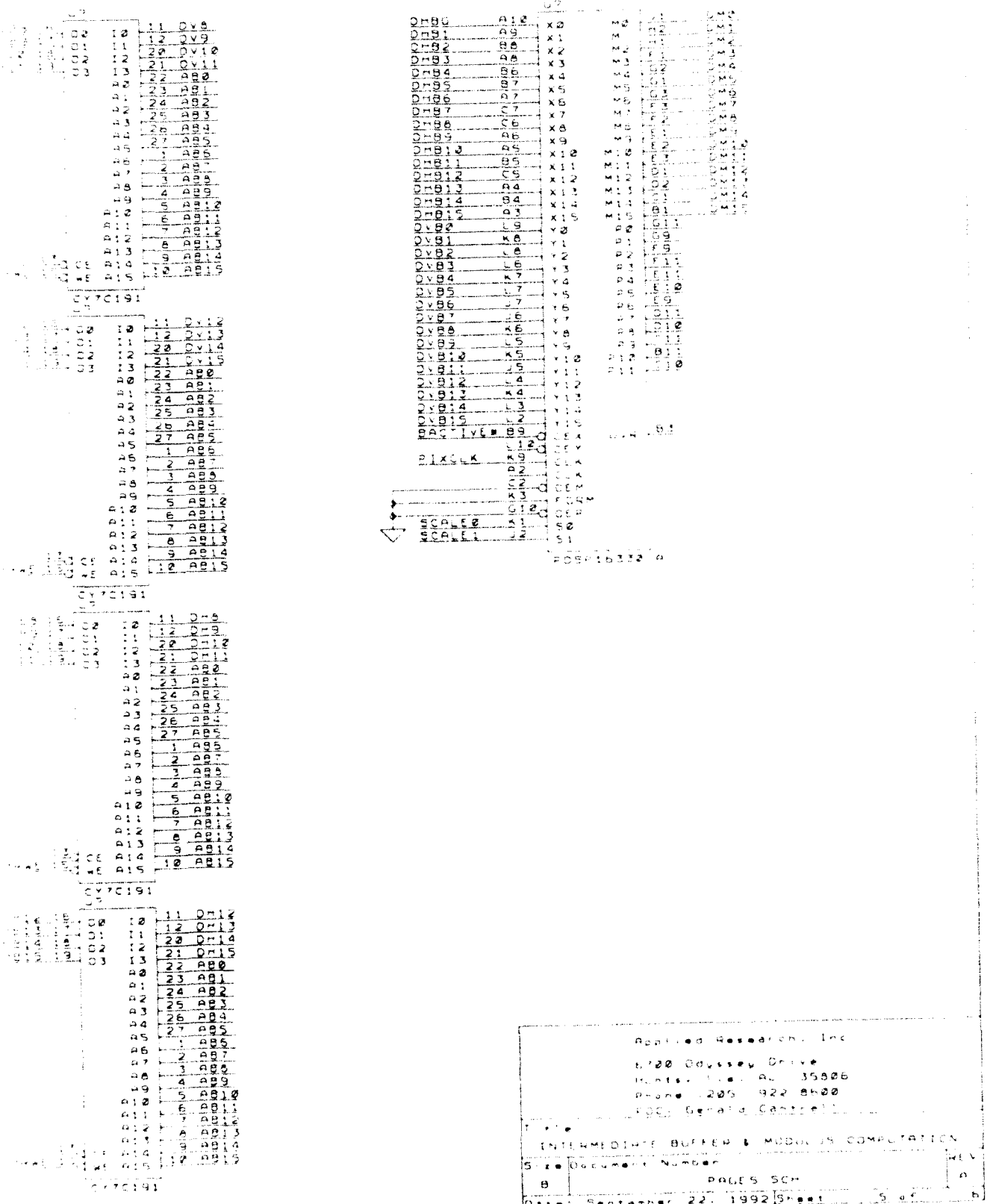

J3
CONNECTOR
B13 IOW#
B14 IOR#
J1
CONNECTOR
A11 AEN#
A12 SA19
A13 SA18
A14 SA17
A15 SA16
J2
CONNECTOR
C10 MEMR#
C9 MEMW#
C8 LA17
C7 LA18
C6 LA19
C5 LA20
C4 LA21
C3 LA22
C2 LA23
J1C
CONNECTOR
A31 SA0
J3B
CONNECTOR
D2 IOCS16#
D18
BUS DECODING PAL
PALCE26V12-25
J1A
CONNECTOR
A9 SD0
A8 SD1
A7 SD2
A6 SD3
A5 SD4
A4 SD5
A3 SD6
A2 SD7
TOE# 19
TDIR 1
U23
74HCT245
J2A
CONNECTOR
C11 SD8
C12 SD9
C13 SD10
C14 SD11
C15 SD12
C16 SD13
C17 SD14
C18 SD15
TOE# 19
TDIR 1
U24
74HCT245
J1B
CONNECTOR
A30 SA1
A29 SA2
A28 SA3
A27 SA4
A26 SA5
A25 SA6
A24 SA7
A23 SA8
ADE# 19
U25
74HCT541
A22 SA9
A21 SA10
A20 SA11
A19 SA12
A18 SA13
A17 SA14
A16 SA15
A15 SA16
ADE# 19
U26
74HCT541
MCOLLOS OUTPUT COUNTERS
PIXCLK
MCEN
U28
74LS461
U29
74LS461
ACTIVE
CSROE#


MODULE 5
RAM
U30
CY7C191
MWE#
MODULE 6
RAM
U34
CY7C191
MODULE 5
RAM
U31
CY7C191
MODULE 6
RAM
U35
CY7C191
U32
74HCT373
U33
74HCT373
Apple Research Inc.
Document Number
PAGE 6 SCH
Date: September 22, 1992
Sheet 4 of 5

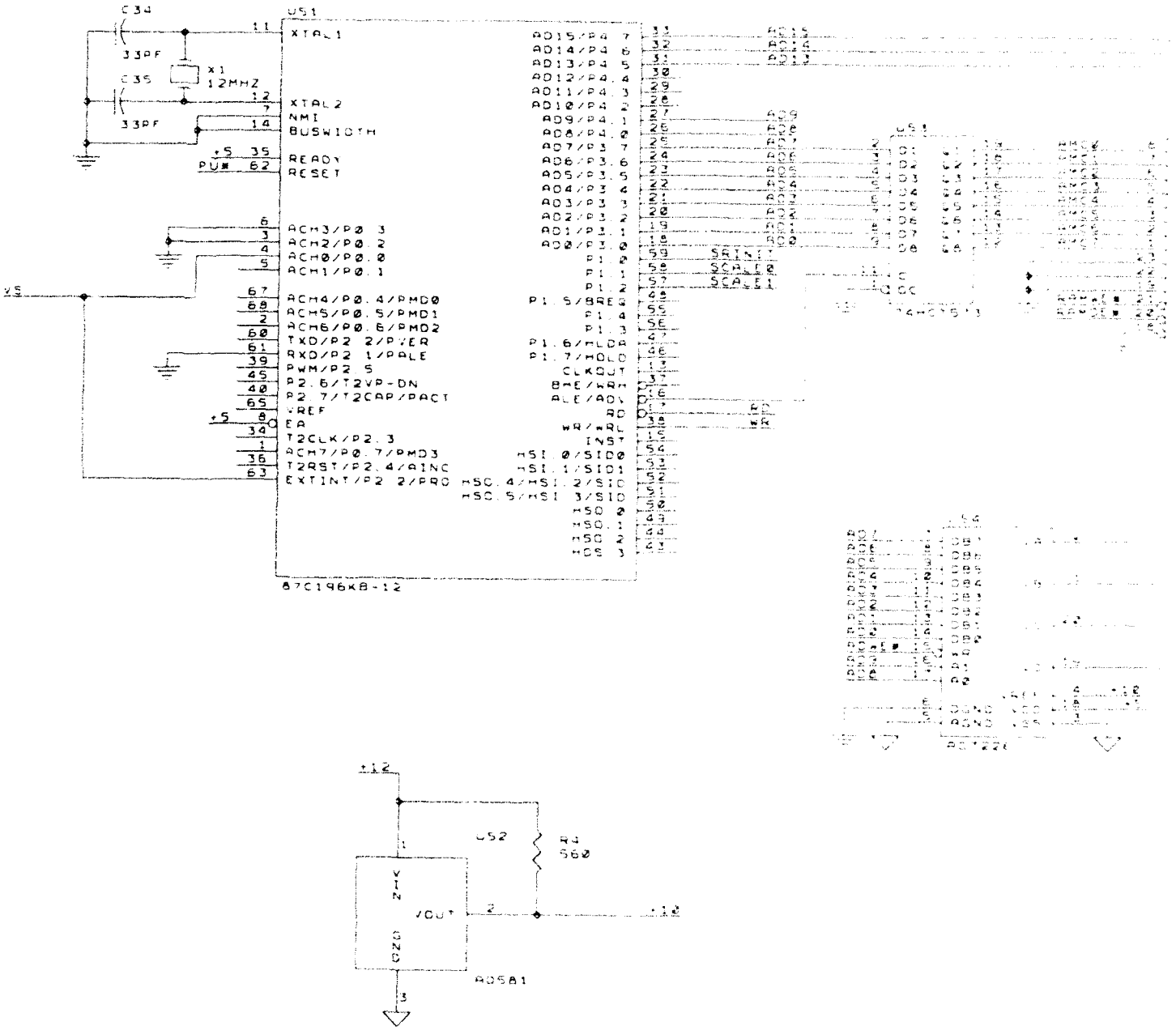

74F579
74F579
PAL22X10
PAL20X10

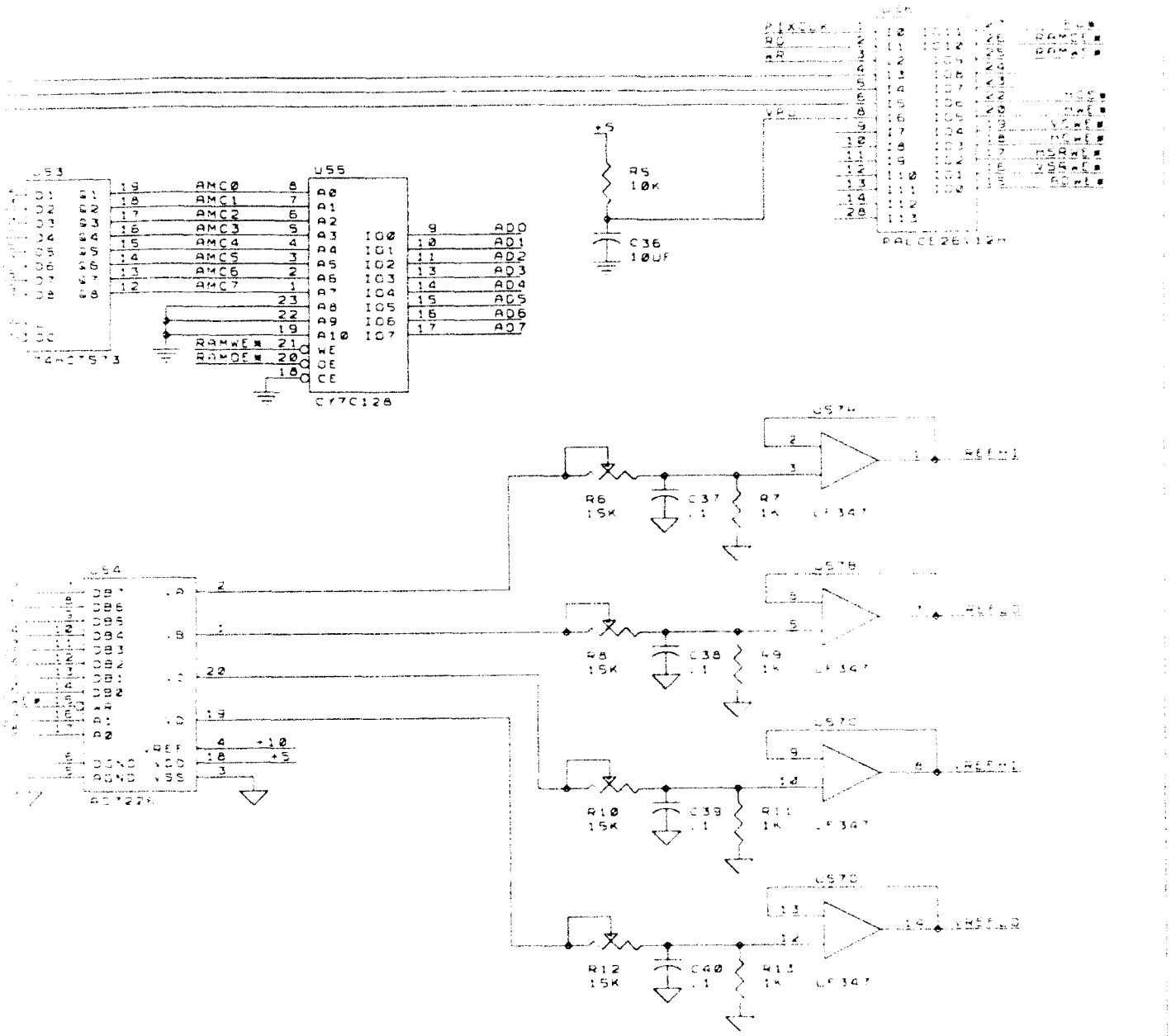






Applied Research, Inc.		
8700 Odyssey Drive		
Huntsville, AL 35806		
Phone (205) 922-8600		
FSC: General Control		
Title: INTERMEDIATE BUFFER & MODULUS COMPLETION		
Size: B	Document Number: PAGES.SCH	REV: B
Date: September 22, 1992	Sheet 5 of 5	

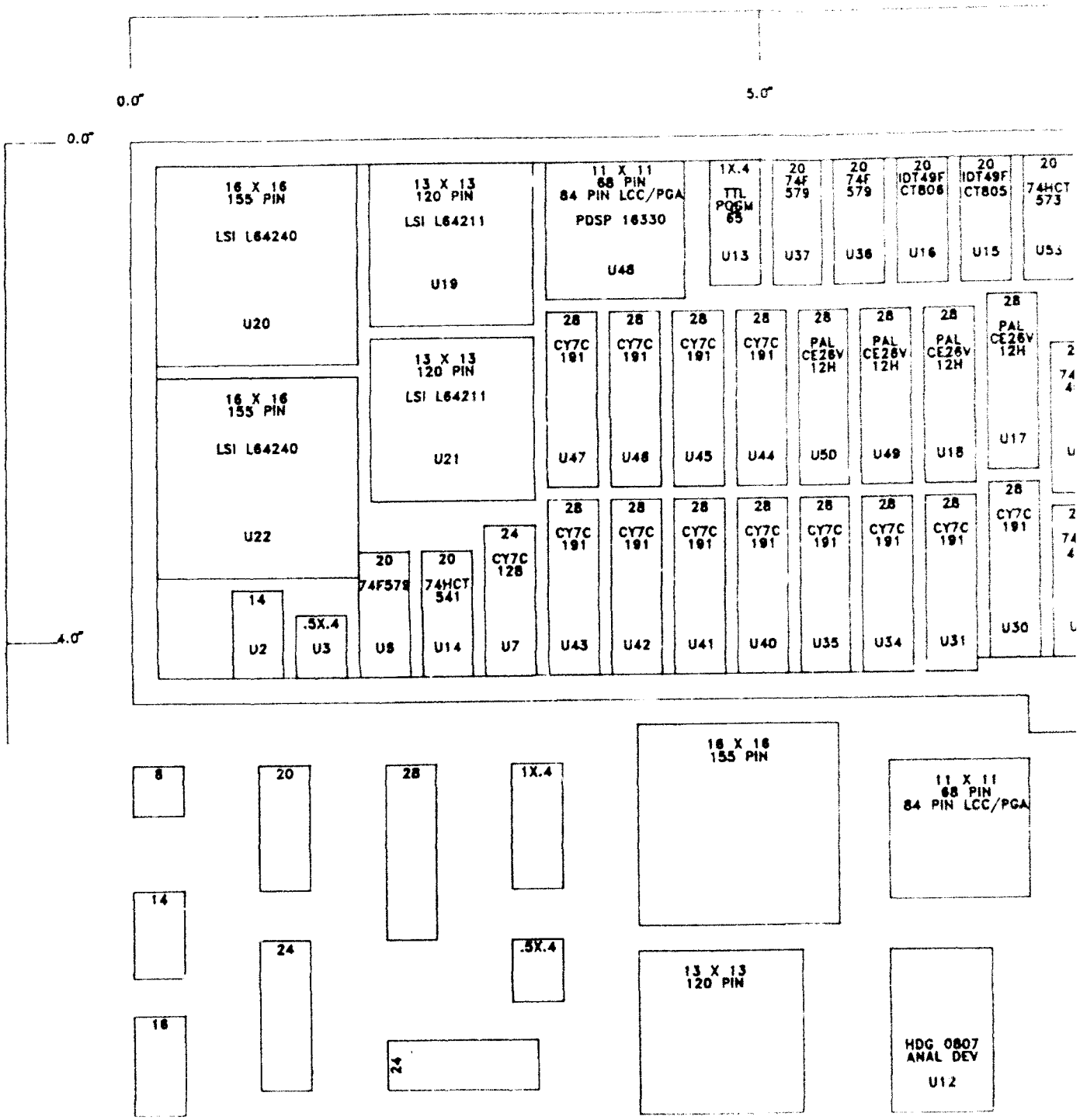

C34
33PF
C35
33PF
X1
12MHZ
U51
XTAL1
XTAL2
NMI
BUSWIDTH
READY
RESET
ACH3/P0.3
ACH2/P0.2
ACH0/P0.0
ACH1/P0.1
ACH4/P0.4/PMD0
ACH5/P0.5/PMD1
ACH6/P0.6/PMD2
TXD/P2.2/PVER
RXD/P2.1/PALE
PWM/P2.5
P2.6/T2VP-DN
P2.7/T2CAP/PACT
VREF
EA
T2CLK/P2.3
ACH7/P0.7/PMD3
T2RST/P2.4/AINC
EXTINT/P2.2/PRO
AD15/P4.7
AD14/P4.6
AD13/P4.5
AD12/P4.4
AD11/P4.3
AD10/P4.2
AD9/P4.1
AD8/P4.0
AD7/P3.7
AD6/P3.6
AD5/P3.5
AD4/P3.4
AD3/P3.3
AD2/P3.2
AD1/P3.1
AD0/P3.0
P1.0
P1.1
P1.2
P1.5/BREQ
P1.4
P1.3
P1.6/HLDA
P1.7/HOLD
CLKOUT
BHE/WRH
ALE/ADS
RD
WR/WRL
INST
HSI.0/SIO0
HSI.1/SIO1
HSO.4/HSI.2/SIO
HSO.5/HSI.3/SIO
HSO.0
HSO.1
HSO.2
HSO.3
87C196KB-12
+5
PU#
XS
SRINT
SCALE0
SCALE1
RD
WR
+12
U52
R4
560
VIN
/OUT
GND
+12
A05B1

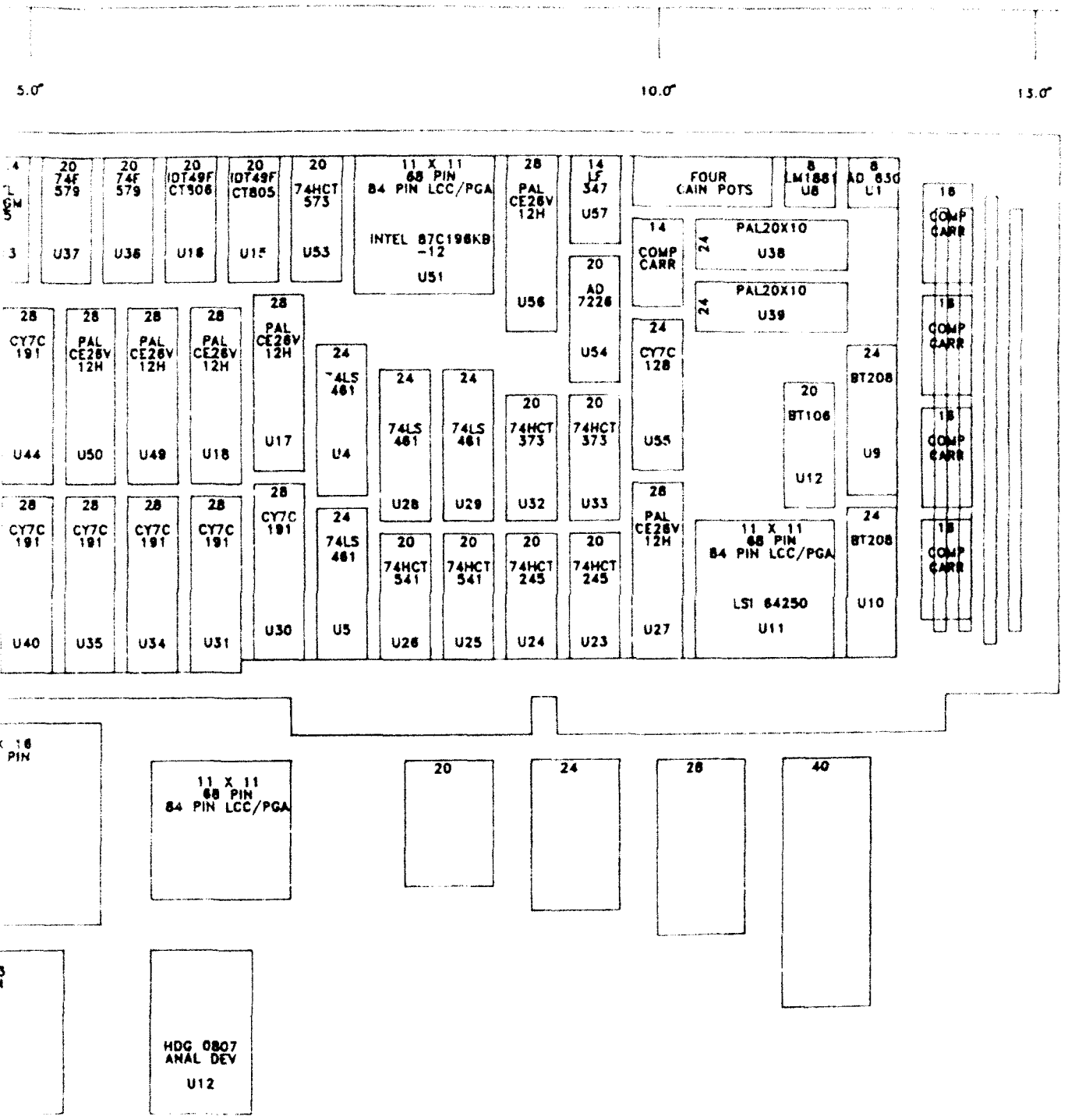


	5700 Odyssey Drive Huntsville, AL 35806 Phone (205) 922-8600 PDCI General Contractor
Title	MICRO CONTROLLER
Size: B	Document Number: PAGE6.SCH — Rev: B
Date: September 22, 1992	Sheet 6 of 6

APPENDIX B

PREPROCESSOR LAYOUT


0.0"
5.0"
0.0"
4.0"
16 X 16
155 PIN
LSI L64240
U20
13 X 13
120 PIN
LSI L64211
U19
11 X 11
68 PIN
84 PIN LCC/PGA
PDSP 16330
U48
1X.4
TTL
PQGM
65
U13
20
74F
579
U37
20
74F
579
U36
20
IDT49F
CT806
U16
20
IDT49F
CT805
U15
20
74HCT
573
U53
16 X 16
155 PIN
LSI L64240
U22
13 X 13
120 PIN
LSI L64211
U21
28
CY7C
191
U47
28
CY7C
191
U46
28
CY7C
191
U45
28
CY7C
191
U44
28
PAL
CE26V
12H
U50
28
PAL
CE26V
12H
U49
28
PAL
CE26V
12H
U18
28
PAL
CE26V
12H
U17
28
CY7C
191
U30
14
U2
.5X.4
U3
20
74F579
U8
20
74HCT
541
U14
24
CY7C
128
U7
28
CY7C
191
U43
28
CY7C
191
U42
28
CY7C
191
U41
28
CY7C
191
U40
28
CY7C
191
U35
28
CY7C
191
U34
28
CY7C
191
U31
8
20
28
1X.4
16 X 16
155 PIN
11 X 11
68 PIN
84 PIN LCC/PGA
14
24
.5X.4
13 X 13
120 PIN
16
24
HDG 0807
ANAL DEV
U12


5.0"
10.0"
15.0"
20 74F 579 U37
20 74F 579 U36
20 IDT49F CT906 U16
20 IDT49F CT805 U15
20 74HCT 573 U53
11 X 11 68 PIN 84 PIN LCC/PGA INTEL 87C196KB -12 U51
28 PAL CE26V 12H U56
14 LF 347 U57
FOUR CAIN POTS
8 LM1881 U8
8 AD 630 U1
16 COMP CARR
14 COMP CARR
PAL20X10 24 U38
PAL20X10 24 U39
20 AD 7226 U54
24 CY7C 128 U55
28 CY7C 191 U44
28 PAL CE26V 12H U50
28 PAL CE26V 12H U49
28 PAL CE26V 12H U18
28 PAL CE26V 12H U17
24 74LS 461 U4
24 74LS 461 U28
24 74LS 461 U29
20 74HCT 373 U32
20 74HCT 373 U33
20 BT106 U12
24 BT208 U9
28 CY7C 191 U40
28 CY7C 191 U35
28 CY7C 191 U34
28 CY7C 191 U31
28 CY7C 191 U30
24 74LS 461 U5
20 74HCT 541 U26
20 74HCT 541 U25
20 74HCT 245 U24
20 74HCT 245 U23
28 PAL CE26V 12H U27
11 X 11 68 PIN 84 PIN LCC/PGA LSI 64250 U11
24 BT208 U10
11 X 11 68 PIN 84 PIN LCC/PGA
20
24
28
40
HDG 0807 ANAL DEV U12